`timescale 1ns / 1ps

module slow\_clock(clk, reset, SlowClk);

input clk, reset;

output SlowClk;

reg SlowClk = 1'b0;

reg [23:0] counter;

always@(posedge reset or posedge clk)

begin

if (reset == 1'b1)

begin

SlowClk <= 0;

counter <= 0;

end

else

begin

counter <= counter + 1;

if ( counter == 10\_000\_000)

begin

counter <= 0;

SlowClk <= ~SlowClk;

end

end

end

endmodule